MSI-P416

DUAL-CHANNEL 16-BIT ISOLATED ANALOG INPUT CARD

USER MANUAL

PC/104 Embedded PC Isolated Industrial Analog I/O Series

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CONTENTS

I. INTRODUCTION

The MSI-P416 is an isolated 16-bit analog input card designed specifically for measuring analog signals in harsh electrical environments in all PC/104 embedded systems. The unit is particularly useful in low frequency measurement applications requiring a high resolution such as those encountered in battery charging, RTU, SCADA, and industrial monitoring and control applications. Commonly encountered ground loop currents and large common-mode voltages associated with analog data acquisition are eliminated by onboard circuitry. The unit is implemented on a 4-layer card using low-power CMOS components for operating in a temperature range from -40°C to 85°C.

The card provides two isolated input channels by using individual onboard dc-to-dc converters for powering the A/D converter, voltage reference, and optocouplers of each channel, as shown in the block diagram of Figure 1. Each power converter also provides a 20 mA source at a minimum

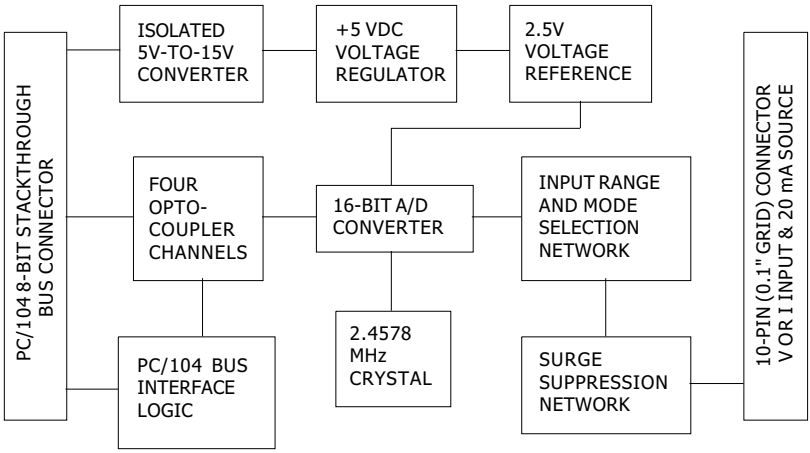

Figure 1. Block diagram of an isolated input channel.

of 14 VDC for exciting transducer transmitters such as thermocouple, RTD, and strain gauge sensors for temperature, pressure, flow, level, and weight measurements. The unique design of the card routes the input analog signals directly to the A/D converter via selectable range resistors and surge suppressor components. This eliminates drift and stability errors of separate intermediate amplifiers for optimum performance. A highly stable reference source provides the span for each channel with a potentiometer adjustment of ±4%.

An Analog Devices AD7715 16-bit sigma-delta A/D converter is used in each input channel. It contains a microcontroller with on-chip static RAM, a clock oscillator, a digital filter and a bi-directional serial communications port. It has a software calibration mode that both zeros and spans (to the reference voltage or to user applied input voltages) at the terminals of the converter. Other programmable functions include gains of 1, 2, 32 and 128; unipolar and bipolar input operation; buffered and unbuffered internal amplifier inputs; and a low-pass filter with output update rate. A full 16-bit conversion accuracy and a 0.0015% nonlinearity are provided for current (mA) and voltage (V) input ranges with 13-bit accuracy for mV ranges. An Analog Devices AD780 provides the voltage reference with 3 ppm/°C maximum drift.

The card is I/O mapped using 16-bit addressing with SA5 thru SA15 specifying the base address of the card. Option jumpers are provided for address selection. The address of the communication register of channel 0 is at the base address and that of channel 1 is at the base address+1. All read and write operations are performed at these addresses.

II. HARDWARE DESCRIPTION

A. Configuration and Functionality.

The MSI-C416 card is a 4-layer CMOS design using through-hole and surface-mounted devices. The card configuration is shown in Figure 2 and a circuit diagram of the network is given in the Appendix. The input signal for channel 0 [1] is applied to connector J1 [J2] (*where* [x] *denotes channel 1 values*). This signal is directed to the input terminals of the A/D converter U16 [U18] (Analog Devices AD7715) via a surge suppression and an input range/mode selection network. The input range is configured by jumpers JP2-JP4 [JP6-JP8] and the unipolar or bipolar mode of operation by JP5 [JP9].

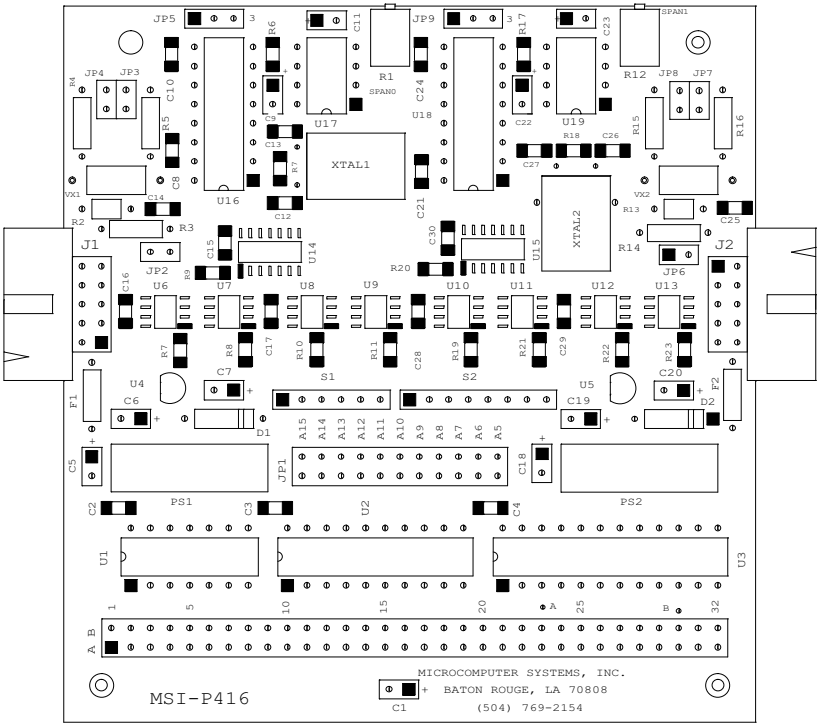

Figure 2. MSI-P416 card outline.

The span of the channel is set by the value of the reference voltage generated by U17 [U19] (Analog Devices AD780). The span is adjustable ±4% by potentiometer R1 [R12]. The input impedance of each channel is approximately 20 kΩ for V ranges and 5.8 kΩ for mV ranges. The potentiometer provides adjustment to accommodate input sources with impedances of up to 1200Ω [350Ω] for V [mV] inputs with a zero span error.

The inputs to the converter from the processor card via the bus interface logic are serial data DIN0 [DIN1] and clock input SCLK0 [SCLK1]. The input signals are passed from U3 (22CV10A) via optocouplers U8-U9 [U12-U13] (Hewlett Packard HCPL0201) that provide the signal isolation. The inputs from the PC/104 bus are then applied directly to U3. Outputs to the processor are serial data out DOUT0 [DOUT1] and a data ready DRDY0* [DRDY1*]. These outputs are applied to U1 (74HCT125) via optocouplers U6-U7 [U10-U11]. The outputs of U1 are then passed to the PC/104 bus.

Sixteen-bit I/O mapped addressing is provided by jumper JP1 which permits selection of addresses SA5 thru SA15. Decoding is performed by a combination of U2 (74HCT688) and U3. The card is selectable on boundaries that are modulo 20H from 0000H to 0FFFFH, where H denotes a hexadecimal number.

The DC-to-DC converter PS1 [PS2] (Burr Brown HPR102) provides an isolated +15VDC supply which operates from the +5V input of the bus. A +5V regulator U4 [U5] (78L05) at the output of the voltage converter provides the excitation for the voltage reference and converter of the channel.

B. Card Addressing.

The card address is set by installing appropriate jumpers on JP1. An uninstalled jumper for a given address bit sets the bit to 0 (false) and an installed jumper sets the bit to 1 (true). Addresses SA5 thru SA15 are selectable which

places the *base address* of the card on integral 20H boundaries. To assign a base address of 3040H, for example, install jumpers JP1-A13, JP1-A12 and JP1-A6.

The input and output addresses of data in (DINx to the converter), data out (DOUTx from the converter), data ready (DRDYx* from the converter), and clock (CLKx to the converter) for each A/D channel x are determined by the base address + SA0 as follows.

SA0	IOR*	IOW*	SD0	SD1
0	0	1	DOUT0	DRDY0
1	0	1	DOUT1	DRDY1
0	1	0	DIN0	CLK0
1	1	0	DIN1	CLK1

Note: IOR*, IOW*, SD0 and SD1 are PC/104 bus signals.

C. Bipolar or Unipolar Input Selection.

The bipolar or unipolar input selection requires a jumper installation for each channel as given below. The bipolar mode permits voltages of ±5V, ±10V and ±50mV. The unipolar mode gives ranges of 0-5V, 0-10V, 0-50 mV and 0-20 mA.

Mode	Channel	Channel 1
Bipolar	JP5-1,2	JP9-1,2
Unipolar	JP5-2,3	JP9-2,3

D. Voltage or Current Input Range Selection.

The voltage or current input range for the card is individually selectable for each channel for either bipolar or unipolar operation. Input voltage ranges are 0-5V, ±5V, 0-10V, ±10V, 0-50 mV and ±50 mV. The current input ranges are and 0-20 mA. Jumper configurations for these input

ranges and the appropriate programmed gain value are given below. The bipolar and unipolar jumpers described previously are also included for completeness.

Input Range	Channel 0 Jumpers	Channel 1 Jumpers	Programmed Gain Value
0-5V	JP5-2,3	JP9-2,3	2
±5V	JP5-1,2	JP9-1,2	2
0-10V	JP5-2,3	JP9-2,3	1
±10V	JP5-1,2	JP9-1,2	1
0-50mV	JP3, JP4, JP5-2,3	JP7, JP8, JP9-2,3	128
±50mV	JP3, JP4, JP5-1,2	JP7, JP8, JP9-1,2	128
0-20mA	JP2, JP5-2,3	JP6, JP9-2,3	2

The above ranges denote standard values normally used in most applications. Other ranges can be obtained for the jumper configurations cited above by employing a different programmed gain value. For example, if a gain value of 32 is programmed for the jumper configuration of the 0-5V range, the range would change to a value given by

New range = (Old range * Old gain)/New gain
= (5 * 2)/32 = 0.313 V

Care should be taken to insure that the input voltage does not exceed ±12V at the input. The surge suppressors VX1 and VX2 of channels 0 and 1 will be saturated and current flow will only be limited by the 2Ω (1/8 W) resistor. This network is used to avoid damaging the A/D converters of either channel in the event of voltage surges.

E. Connecting Inputs to J1 and J2.

Signal inputs are applied via connectors J1 and J2 for channels 0 and 1, respectively. The connectors are AMP 103311-1 or equivalent. Each connector provides for differential inputs and isolated 20 mA (fused at 62 mA) output sources at +14V minimum for powering transducer transmitters. The pin connections are the following.

Channel	+In Pin/Signal	-In Pin/Signal	Isolated Ground	Isolated 20mA Source
0	J1-9/VIN0+	J1-7/VIN0-	J1-5	J1-2
1	J2-1/VIN1+	J2-3/VIN1-	J2-5	J2-10

Note: All other pins have no connections.

F. Using the Isolated 20 mA Sources.

The isolated 20 mA sources are useful for exciting sensor loops that contain no power supply. The recommended connection for these elements is shown in Figure 3. When using this arrangement, the jumper configuration is set as specified for 0-20mA operation (see Sec. II-D).

The current sources eliminate the need for an external power source to supply loop current for the channel input. The sources are useful for powering transmitters for thermocouple, RTD, pressure, flow, level, and deformation type transducers.

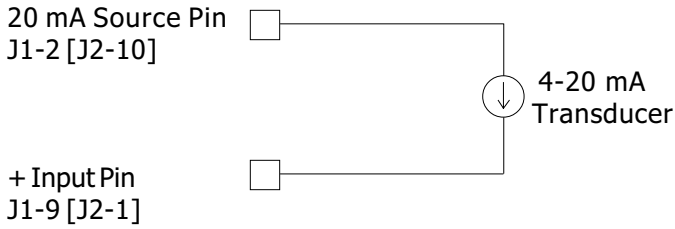

Figure 3. Connection for 20 mA isolated current source.

III. PROGRAMMING

The A/D converter contains four registers that are accessed using data bit 0 (SD0) obtained using the base address and base address+1 for channels 0 and 1, respectively. A data bit is written by setting bit 0 to the desired value followed by toggling the clock bit to 0 and then to 1. The clock bit is accessed by data bit 1 (SD1) of the base address and base address+1 for channels 0 and 1, respectively. Byte transfers are performed by executing eight sequential bit writes beginning with the most-significant-bit (MSB). Data reads are performed in a similar manner by setting the clock bit to 0, reading data bit 0, and then setting the clock bit to 1. Byte or word transfers are executed by eight or sixteen sequential bit reads beginning with the MSB. Reading data bit 1 (SD1) of the desired channel provides DRDYx* directly. No clock operation is required.

Registers of each converter consist of the Communications Register, the Setup Register, the Data Register, and the Test Register, henceforth, to be referred to as C Reg, S Reg, D Reg and T Reg, respectively, for the sake of brevity.

A. Communcations Register (C Reg)

C Reg is an 8-bit register which can either be read or written. All communications to the converter must start with a write operation to C Reg. The data written defines whether the next operation is a read or write and in which register this operation takes place. Once the sequential read or write to the selected register is complete, the interface returns to the state expecting a write to C Reg. This is the default state of the converter, and on power-up, it is in this state awaiting a write to C Reg. The bit designations of C Reg are

Bit 7	6	5	4	3	2	1	Bit 0
0/DRDY*	ZERO	RS1	RS0	R/W*	STBY	G1	G0

where the bits are defined as follows.

0/DRDY* - For a write operation, a 0 must be written to this bit. If a 1 is written, no operation occurs. For a read operation, this bit provides the status of the DRDY* flag of the converter which is the same as the DRDY* output pin. (It is recommended that the status of the device be determined by reading DRDYx* of DS1 as described above).

ZERO - For a write operation, a 0 must be written to this bit. For a read operation, a 0 will be read from this location.

RS1, RS0 - Register Selection Bits. Selects the register for the next read or write operation.

RS0	RS1	Register	Register Size
0	0	C Reg	8 Bits
0	1	S Reg	8 Bits
1	0	T Reg	8 Bits
1	1	D Reg	16 Bits

R/W* - Read/Write Select. This bit selects whether the next operation is a read or write. A 0 indicates a write cycle as the next operation and a 1 indicates a read operation as the next operation.

STBY - Standby. Writing a 1 to this bit places the converter in its standby or power-down mode in which the part consumes only 10 uA of supply current. Writing a 0 places the converter in its normal operating mode. The default at power-on is 0.

G1, G0 - Gain Bits. Selects the gain setting of the converter.

G1	G0	Gain Setting
0	0	1
0	1	2
1	0	32
1	1	128

B. Setup Register (S Reg)

The S Reg is an 8-bit register which can either be read or written. It controls the setup which specifies the converter operation such as calibration, output rate, unipolar/ bipolar mode, etc. The bit designations for S Reg are given below.

Bit 7	6	5	4	3	2	1	Bit 0
MD1	MD0	CLK	FS1	FS0	B*/U	BUF	FSYNC

where the bits are defined as follows.

MD1,MD0 - Operating Mode Bits.

MD1	MD0	Operating Mode
0	0	Normal mode of operation in which the device is performing conversions. This is the default power-on value.
0	1	Self-Calibration mode is a one step sequence and when completed the device returns to the normal mode of operation with MD1 and MD0 equal 0. The DRDY* output or bit becomes 1 when calibration starts and returns to 0 upon completion and when a new valid conversion is in D Reg. The zero-scale calibration is performed at the selected gain on internally shorted inputs and the full-scale calibration at the selected gain on an internally generated Vref/Selected Gain.
1	0	Zero-Scale System Calibration mode activates a zero-scale system calibration on the converter. Calibration is performed at the selected gain on the analog voltage placed at the analog input during the calibration sequence. This voltage should remain stable during the calibration sequence. The DRDY* output or bit becomes 1 when calibration starts and returns to 0 upon completion and when a new valid conversion is in D Reg. At the end of the calibration, the converter returns to the normal mode of operation with MD1 and MD0 equal 0.
1	1	Full-Scale System Calibration mode activates a full-scale system calibration on the converter. Calibration is performed at the selected gain on the analog voltage placed at the analog input during the calibration sequence. This voltage should remain stable during the calibration sequence. The DRDY* output or bit becomes 1 when calibration starts and returns to 0 upon completion and when a new valid conversion is in D Reg. At the end of the calibration, the converter returns to the normal mode of operation with MD1 and MD0 equal 0.

CLK - Clock BIt. This bit must be set to 1 for the MSI-P416. The default value at power-on is 1.

FS1, FS0 - Filter Selection Bits. Determines the output update rate, filter

first notch and -3 dB frequency.

FS1	FS0	Output Update Rate	-3dB Filter Cutoff
0	0	50 Hz	13.1 Hz
0	1	60 Hz	15.7 Hz (Default)
1	0	250 Hz	65.5 Hz
1	1	500 Hz	131.0 Hz

B*/U - Bipolar/Unipolar Operation Bit. A 0 selects bipolar operation which is the power-on default value. A 1 selects unipolar operation.

BUF - Buffer Control. When this bit is 0, the converter buffer amplifier is shorted out, implementing the unbuffered mode. The MSI-P416 is designed to operate in this mode so that the surge suppression network on the input of each channel can function properly. When the bit is 1, the buffer amplifier is placed in series with the analog input. This permits higher source impedances associated with the input analog voltage; however, an offset voltage of 50 mV is introduced. In addition, the maximum input voltage with respect to ground is reduced from 5V to 3.5V which limits the full-scale operation in the bipolar mode.

FSYNC - Filter Synchronization Bit. When this bit is 1, the converter is held in a reset state. When the bit changes to 0, a valid word is available in D Reg in 3 x 1/(output update rate). The bit does not reset DRDY* if it is low.

C. Test Register (T Reg)

The T Reg is an 8-bit test register used in testing the device. The register must always contain 0's. If a test mode is accidentally entered, the part can be reset by writing 32 successive 1's followed by writing 8 0's to T Reg (see Sec. III-E). The power-on default for T Reg is all 0's.

D. Data Register (D Reg)

The D Reg is a 16-bit read-only register that contains the most up-to-date conversion result of the converter. If a write operation is initiated, the write must be completed (i.e., 16 clocks sent) to return the part to the condition of awaiting a write operation to C Reg. The 16 bits of data written, however, are ignored by the converter.

E. Example Program

Programming the MSI-P416 requires initializing both channels for the desired configuration and then reading the channels for the converted data. The steps required for each channel for unipolar operation are the following.

1. Initialize the AD7715.
   a) Determine the value of C Reg required to write T Reg. Call it TEST_W for convenience.
   b) Perform a software reset by sending 32 successive 1's (4 bytes equal to 0FFH) to the converter followed by 8 successive 0's (1 byte equal to 0) to T Reg. The write to T Reg is performed by writing TEST_W to select T Reg followed by the 0 byte write. This places the converter into the default power-on state. Steps (a) and (b) are optional (but recommended) at power-on.
   c) Determine the value of C Reg required to write S Reg. Call it SETUP_W for convenience.
   d) Determine the value of S Reg required to perform a Self-Calibration. Call if CALIBRATE_W.
   e) Write SETUP_W to the converter to select S Reg for a write operation.
   f) Write CALIBRATE_W to the selected S Reg to perform a self-calibration operation on the converter.
2. Read converter data.
   a) Test the DRDY* pin for data available. The MSI-P416 hardware interface is designed so that DRDY* is read directly from DS1 at the converter address. If DRDY* is 0 data is ready, proceed to the next step (2-b).
   b) Determine the value of C Reg required to read D Reg. Call if DATA_R.
   c) Write DATA_R to the converter to select D Reg for a 16-bit read operation.

d) Perform a 16-bit read operation.

e) Repeat the read operation beginning at step 2-a.

Suppose one wishes to use the converter for an application in which channels 0 and 1 are configured for 0-5V operation. This requires the following parameters.

Gain = 2: G1 = 0, G0 = 1
Unipolar Mode: B*/U = 1

Therefore, TEST_W = 00100001B = 21H (where B denotes a binary number), SETUP_W = 00010001B = 11H, CALIBRATE_W = 01101100B = 6CH and DATA_R = 00111001B = 39H. A simple C language program that performs the functions of the above step sequence is given below. The routines get_ready_status, send_BYTE, get_BYTE, reverse_BYTE, and init_7715 should be very useful in developing user applications.

```
/* Sample Program for MSI-P416 configured for 0-5V operation */
/* Program initializes and reads Ch 0 & Ch 1 and prints value */
/* to console. Requires jumpers JP5-2,3 and JP9-2,3 */

#include <dos.h>
#include <stdio.h>
#include <conio.h>
#include <graph.h>

/* Card Addresses */

#define BASE_ADDR 0x3000 //Assign a base address of 3000H
                         // Install jumpers J1-A12, A13
/* Register Parameters */

#define TEST_W      0x21  //Write test  "   "   "
#define SETUP_W     0x11  //Write setup "   "   "
#define DATA_R      0x39  //Read data   "   "   "
#define CALIBRATE_W  0x6c  //setup data for self calibration
                           //unbuffered in unipolar mode
/* Memory allocations */

int setup_wr, test_wr, data_rd, calibrate_data;
unsigned int addr0, addr1;

/* Program Routines */

void send_BYTE( int x, int a_byte )  // write a_byte to Ch x
{                                    // (x = 0 or 1)
    int a, i;
    unsigned int adr;
```

```
    if (x == 0) adr = addr0;
    else adr = addr1;
     a = 0;
    for (i = 8; i>0; --i)  // perform write operation
     {
        a = (a & 0xfc) | (a_byte & 1); // SCLKx=0 (bit 1) + data bit
         a_byte >>= 1;                 // get bit to xmit in position 0
         outp(adr, a);                 //set SCLKx lo
         a = a | 2;
         outp(adr, a);                 //set SCLKx hi
     }
    outp(adr, 3);
}

int get_BYTE( int x )  // return a BYTE read from Ch x (x = 0 or 1)
{
    int a, b, i;
    unsigned int adr;

    if (x == 0) adr = addr0;
    else adr = addr1;
     b=0;
    for (i = 8; i>0; --i)       //perform read operation
     {
        outp(adr, 1);        //SCLKx lo
        a = inp(adr);       //input data bit DOUT of 7715
         b <<= 1;
         b = (a & 1) | b;
         outp(adr, 3);       //SCLKx hi
     }
    return (b);
}

int get_ready_status( int x ) //get !DRDYx for Ch x (x= 0 or 1)
{                             //Return a = -1 if valid status.
     int a;
    unsigned int adr, delay;

    if (x == 0) adr = addr0;
    else adr = addr1;
     delay = 0xffff;         // set timeout to maximum value
      do
      {
          --delay;
         a = inp(adr) & 0x2;
    }while ((a > 0) && (delay > 0));// wait till !DRDYx is LO
    if(delay == 0) a = 0;
    else a = -1;
     return( a );
}

void init_7715( int x )  //initialize 7715 Ch x (x = 0 or 1)
{
     int a, i;
    unsigned int adr;

    if (x == 0) adr = addr0;
    else adr = addr1;
   get_BYTE(x); get_BYTE(x); get_BYTE(x); get_BYTE(x);  // receive 24 bits
     send_BYTE(x,0xff); send_BYTE(x,0xff);                  // send 32 1's
   send_BYTE(x,0xff); send_BYTE(x,0xff);
     send_BYTE(x,test_wr);              // point at Ch x test reg
```

```
    send_BYTE(x,0);                    // write 0's
    send_BYTE(x,setup_wr);             // point at setup reg
    send_BYTE(x,calibrate_data);       //start self calibation
    get_ready_status(x);
}

int reverse_BYTE( int a_BYTE ) // routine to the reverse order of
                               // a_BYTE and shift result 1 bit
{                                 // to the left.
    int a, i;

    a = 0;
    for (i = 8; i>0; --i)          // reverse order of a_BYTE
    {
       a = (a & 0xfe) | (a_BYTE & 1);
       a_BYTE >>= 1;
        a <<= 1;
    }
    a >>= 1;
    return( a );
}
void main( void )
{
   int a, b, c, d, e;

   addr0 = BASE_ADDR;      //Ch 0 address
   addr1 = BASE_ADDR + 1;   //Ch 1 address
   test_wr = reverse_BYTE(TEST_W);//reverse byte bits
   setup_wr = reverse_BYTE(SETUP_W);
   calibrate_data = reverse_BYTE(CALIBRATE_W);
   data_rd = reverse_BYTE(DATA_R);
    init_7715(0);          // init Ch 0
    init_7715(1);          // init Ch 1
a0:  while(!kbhit());
    d=getch();
    if(d==0x43)
     {
       send_BYTE(0,setup_wr);//point at setup reg
      calibrate_data=reverse_BYTE(CALIBRATE_W|0xc0);
       send_BYTE(0,calibrate_data);
     }
    d = get_ready_status(0);    //get Ch 0 status
    if (d)
    {
      send_BYTE(0, data_rd); //point at R Reg Ch 0
       b = get_BYTE(0);     //get hi byte of Ch 0
       c = get_BYTE(0);     //get lo byte
      printf("\n %x %x",b,c); //print Ch 0 on console
    }
   d = get_ready_status(1);    //get Ch 1 status
    if (d)
    {
      send_BYTE(1, data_rd); //point at R Reg Ch 1
       b = get_BYTE(1);     //get hi byte of Ch 1
       c = get_BYTE(1);     //get lo byte
      printf("\n %x %x",b,c); //print Ch 1 on console
    }
    goto a0;
}
//EOF
```

F. Calibration Procedures

The AD7715 provides a number of options that can be programmed using the MD0 and MD1 bits of S Reg. These calibration options are described below.

1. Self-Calibration (MD1 = 0, MD0 = 1)

The self-calibration is initiated by writing the values MD1 =0 and MD0 = 1 to S Reg. In this mode, with a unipolar input, the zero-scale point used in determining the calibration coefficients with the inputs of the differential pair internally shorted. The gain of the converter is set for the selected gain corresponding to the G1 and G0 bits of C Reg. The full-scale calibration conversion is then performed at the selected gain on an internally generated voltage of Vref/Selected gain, where Vref is nominally 2.5V. The MD1 and MD0 bits of S Reg are set equal to 0. The DRDY* pin = 1 when the calibration begins and returns to 0 when completed with a new word in D Reg. The duration of the calibration from DRDY* = 1 until DRDY* = 0 is

$$t_{cal} = 9/\text{Output Rate}$$

For the bipolar mode the sequence is very similar to that for the unipolar case. The two calibration points are exactly the same, but since the part is configured for bipolar operation, the shorted inputs point is actually midscale of the input voltage range.

The calibration is performed by adjusting the span potentiometer (R1 of Ch 0 or R12 of Ch 1) until the converter produces a full scale output of FFFFH. This is the recommended calibration mode if the offset and span values for the application are satisfied. If not, the system calibration method described below should be employed.

The MSI-416 input impedance is designed for a minimum of 20 kΩ for voltage and 5.8 kΩ for mV input ranges. Input sources having internal impedances up to 1200Ω and

350Ω, respectively, for the voltage and mV input ranges are accommodated by the span potentiometers and provide a zero span error.

2. System Calibration

System calibration allows the converter to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration but uses voltage values presented to the converter inputs for the zero- and full-scale points. Full system calibration, in general, requires a two step process, a ZS System Calibration followed by a FS System Calibration.

a) ZS System Calibration (MD1 = 1, MD0 = 0).

The ZS System Calibration first requires applying the zero-scale voltage to the terminals of the desired input channel. During calibration, this voltage must remain stable. The calibration is then initiated by writing the values MD1 = 1 and MD0 = 0 to S Reg. The zero-scale system calibration is performed and the MD1 and MD0 bits of S Reg are set equal to 0. The DRDY* pin = 1 when calibration begins and returns to 0 upon completion with a new word in D Reg. The duration of the calibration from DRDY* = 1 until DRDY* = 0 is

$$t_{cal} = 4/\text{Output Rate}$$

a) FS System Calibration (MD1 = 1, MD0 = 1).

The FS System Calibration first requires applying the full-scale voltage to the terminals of the desired input channel. During calibration, this voltage must remain stable. The calibration is then initiated by writing the values MD1 = 1 and MD0 = 1 to S Reg. The full-scale system calibration is performed and the MD1 and MD0 bits of S Reg are set equal to 0. The DRDY* pin = 1 when calibration begins and

returns to 0 upon completion with a new word in D Reg. The duration of the calibration from DRDY* = 1 until DRDY* = 0 is

$$t_{cal} = 4/\text{Output Rate}$$

In the unipolar mode, the system calibration is performed between the endpoints of the zero- and full-scale values whereas in the bipolar mode, it is performed between mid- and full-scale values. Since the system calibration is a two-step calibration, after a full-system calibration is completed, additional offset (ZS) or gain (FS) calibrations can be performed independently to adjust the zero reference point or the system gain. In either case, calibrating one parameter does not affect the other.

3. Span and Offset Limits

Whenever a system calibration mode is used, there are limits on the amount of offset or span that can be accommodated. The primary requirement of the amount of offset or gain that can be accommodated is that the

$$\text{Positive Full-scale Calibration Limit} \leq \text{Vref/Gain}$$

where Vref = 2.5V for the MSI-P416.

The range of input span in both the unipolar and bipolar modes is

$$0.8\ \text{Vref/Gain} \leq \text{Span} \leq 2.1\ \text{Vref/Gain}$$

In both unipolar and bipolar modes, the range of positive offsets that can be handled by the converter depends on the selected span. Therefore, in determining the limits for system zero- and full-scale calibrations, one must ensure that

$$\text{Offset} + \text{Span} \leq 1.05\text{Vref/Gain}$$

G. Software Support

Software support is included on the diskette labelled MSI-P416 Software Support which includes a demo program, P416.C (and executable file P416.EXE), written in C language. This program provides useful C Reg, S Reg, T Reg and D Reg bit definitions for various operating modes, update rates, etc. In addition, illustratives routines are provided which should be useful in development of user applications.

The executable file P416.EXE can be run for evaluating the functionality of the card for all of the available input ranges in either the unipolar or bipolar modes.

IV. SPECIFICATIONS

PC/104	8-bit, stackthrough
Analog Inputs	
Channels	Two differential input
Converter	Analog Devices AD7712AN-5
Input Ranges	0-5V, ±5V, 0-10V, ±10V, 0-50mV, ±50mV, 0-20mA
Conversion Rate	60 per second
Isolation Voltage	750 V input-to-input 750 input-to-PC/104 bus
Resolution	16-bit for V and mA ranges 13-bit for mV ranges
Accuracy	±1 LSB
Non-linearity	0.0015%
Input Impedance	20 KΩ min., voltage ranges 5.8 KΩ min., mV ranges 249 Ω, mA ranges
CMR	95 dB minimum 150 dB minimum @ 60 Hz
Coding	Binary
Surge Suppressor	TVS/capacitor with series 2 Ω (1/8W) resistor
Connectors	AMP 103311-1 or equiv. (10-pin, 0.1" grid)
Current Sources	20 mA @ 14 VDC minimum
Voltage References	
Type	Analog Devices AD780BN
Drift	3 ppm/° C maximum
Noise	100nV/(Hz)1/2
Optocouplers	
Type	Hewlett-Packard HCPL0201
DC/DC Converters	
Type	Burr-Brown HPR102
Addressing	16-bit I/O mapped using SA5 thru SA15.

Option Jumpers .025" square posts, 0.1" grid

Electrical & Environmental

+5V @ 200 mA typical
-40° to 85° C

APPENDIX